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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,961	01/28/2004	Dominique P. Bonneau	FR920020088US1	1960

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INTELLECTUAL PROPERTY LAW
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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,961	BONNEAU ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *06/19/06*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election / Restriction

Restriction to one of the following invention is required under 35 U.S.C. 121

Group I: Claims **1-8,** drawn to: A serializer/deserializer (SERDES) circuit having built-in self-test (BIST) capabilities that is configured to perform jitter sensitivity characterization, comprising a CDR circuit coupled to said SERDES circuit that generates recovered clock and data from an incoming serial data stream, a deserializer circuit connected to said CDR circuit to generate corresponding data (Parallel Data Out) and clock (DES clock) in a programmable pattern generator generating BIST patterns; a serializer circuit that receives either the a parallel format, BIST patterns or the input data (Parallel Data In) in a parallel format on its data input and an external clock (SER clock) on its clock input to generate a serial data stream, a delay perturbation circuit for adding a perturbation delay to said serial data stream to produce a perturbed serial data stream; a multiplexor circuit to output either the serial data stream or the perturbed serial data stream in a loop back to the CDR circuit; a control logic circuit block coupled to said deserializer circuit to detect a start-of-frame pattern using a dedicated signal (FD) and coupled to the programmable pattern generator and the perturbation circuit (as in claim 1) classified in 714/738.

Group II: Claims **9-11,** drawn to: A method of characterizing the jitter sensitivity of a clock and data recovery (CDR) circuit connected in series with a deserializer circuit within a serializer/deserializer (SERDES) circuit having built-in self-test (BIST)

capabilities comprising the steps of generating a serial data stream by the serializer that is continuously applied to the CDR circuit and the deserializer; inserting a first start-of-frame pattern in the serial data stream; adding a perturbation delay to said serial data stream to produce a perturbed serial data stream, inserting a second start-of-frame pattern in the serial data stream, and determining whether the deserializer has detected whether said second start-of-frame pattern has the same bit alignment as the first start-of-frame pattern (as in claim 9) classified in 714/733.

The invention are distinct, each from the other because of the following reasons: Invention Group I and group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable.

In the instance case, invention Group I has separate utility separate utility such as a serializer/deserializer (SERDES) circuit comprising a deserializer circuit connected to said CDR circuit to generate corresponding data (Parallel Data Out) and clock (DES clock) in a programmable pattern generator generating BIST patterns; a serializer circuit that receives either the a parallel format, BIST patterns or the input data in a parallel format on its data input and an external clock on its clock input to generate a serial data stream, a delay perturbation circuit for adding a perturbation delay to said serial data stream to produce a perturbed serial data stream, a multiplexor circuit to output either the serial data stream or the perturbed serial data stream in a loop back to the CDR circuit, a control logic circuit block coupled to said deserializer circuit to detect a start-of-

frame pattern using a dedicated signal (FD) and coupled to the programmable pattern generator and the perturbation circuit.

In the instant case, the invention of Group II has separate utility such as a method of characterizing the jitter sensitivity of a clock and data recovery (CDR) circuit connected in series with a deserializer circuit within a serializer/deserializer (SERDES) circuit having built-in self-test (BIST) capabilities comprising the steps of inserting a first start-of-frame pattern in the serial data stream; adding a perturbation delay to said serial data stream to produce a perturbed serial data stream, inserting a second start-of-frame pattern in the serial data stream, and determining whether the deserializer has detected whether said second start-of-frame pattern has the same bit alignment as the first start-of-frame pattern.

Because these inventions are distinct for the reason given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the reasons given above and search required for Group II is not for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because or their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

A telephone call was made to Robert Walsh on 06/19/06 to request an election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement is traversed (37 CFR 1.143).

Applicant is reminded that upon cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the specification. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

1. Claims **1-8** are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority ((European patent office, EPO) 03368048.9 05/27/03) under 35 U.S.C. 119(a)-(d).

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3.1 Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "the disclosure defined by this invention," "the disclosure describes," etc.

3.11. The **abstract** of the disclosure is objected to because the abstract exceeds 150 words. Correction is required. See MPEP j 608.01(b).

Claim objections

4. Claims **1, 5 and 6** are objected to because of the following informalities:

a) Please define the full word of a written word or phrase for the abbreviations **"CDR"** as specified in the specification (see line 4 of claim 1).

b) Please define the full word of a written word or phrase for the abbreviations **"DLL"** as specified in the specification (see claim 5 and 6).

c) The claims are objected to because the lines for the claim limitations are not indented properly, making reading and entry of amendments difficult. Substitute claims with a proper indentation and lines one and one-half or double spaced on good quality paper are required. (See 37 CFR 1.52(b)).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U. S. C 112

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims **1 and 7** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Claim 1 recites "the input data" instead of "an input data" (see line 13 of claim 1). Therefore, the recitation lacks an antecedent basis.

a) Claim 7 recites "the serializer" instead of "a serializer" (see line 4 of claim 7). Therefore, the recitation lacks an antecedent basis.

Allowable subject matter

6. Claims **1 and 5-7** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Examiner's statement for reason for allowance

7. Claims **1-8** have been allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior art, Payne (U.S. PN: 6,865,222) of record teach an integrated circuit (12) includes a phase locked loop (PLL) (31), a serializer circuit (32) of known configuration, and a built-in self test (BIST) circuit (33) whereby the inputs to the integrated circuit (12) include a reference clock input receives a reference clock signal and further the inputs to the integrated circuit (36) further include a parallel data input (37) which accepts 7-bit words, and a built-in self test circuit enable (BISTEN) signal input (38) (see col. 3, lines 31-40 and abstract). The prior art, Ramamurthy et al. (U.S. PN: 5,790,563) of record teach an integrated circuit 10 has a transmitter (12) and a receiver (14), a serializer 16 associated with the transmitter (12) and a deserializer (18) associated with the receiver (14). The serializer provides specialized functions for converting incoming data from several data streams (as from a parallel input or several serial inputs) into a single serial output. The deserializer (16) separates a single serial input (22) into divergent outputs. Further, Ramamurthy teach a pattern generator (24) provides a (20) bit output through a pattern generator output signal path (26) to a multiplexor (28). However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious a serializer/deserializer (SERDES) circuit having built-in self-test (BIST) capabilities that is configured to perform jitter sensitivity characterization, comprising a CDR circuit coupled to said SERDES circuit that

generates recovered clock and data from an incoming serial data stream, a deserializer circuit connected to said CDR circuit to generate corresponding data (Parallel Data Out) and clock (DES clock) in a programmable pattern generator generating BIST patterns; a serializer circuit that receives either the a parallel format, BIST patterns or the input data (Parallel Data In) in a parallel format on its data input and an external clock (SER clock) on its clock input to generate a serial data stream, a delay perturbation circuit for adding a perturbation delay to said serial data stream to produce a perturbed serial data stream; a multiplexor circuit to output either the serial data stream or the perturbed serial data stream in a loop back to the CDR circuit; a control logic circuit block coupled to said deserializer circuit to detect a start-of-frame pattern using a dedicated signal (FD) and coupled to the programmable pattern generator and the perturbation circuit. Consequently, claim 1 is allowed over the prior art.

Claims **2-8,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 5,790,563 Ramamurthy et al.

US PN: 6,865,222 Payne

US PN: 6,215,835 Kyles

US PN: 6,658,363 Mejia et al.

US PN: 6,725,408 Cao et al.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

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Art unit: 2133

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